REMARKS

Claim Rejections 35 U.S.C. § 103 (a)

Claims 26 and 28

The Examiner has rejected claims 26 and 28 under 35 U.S.C. §103 (a) as being unpatentable over Tsuji (JP 08-204136) and Ito et al. (US 5,847,466).

Applicant respectfully disagrees with the Examiner.

Applicant has amended claim 26. Claim 26, as amended, of the present invention claims a device having I/O connections to a package or board including: a first set of vias located over a first line; a second set of vias located over a second line; a bond pad disposed over the first set of vias and the second set of vias, the bond pad having two or more segments, the segments having the same shape, wherein each of the segments is electrically connected to the first set of vias and the second set of vias, and a wire lead attached directly to the segments. See Figure 4, Figure 5, lines 10-15 on page 7, and lines 12-13 on page 10 of the specification for support for the elements of the claim.

However, neither Tsuji nor Ito et al. teaches a first set of vias located over a first line and a second set of vias located over a second line wherein each segment of a bond pad is electrically connected to the first set of vias and the second set of vias.

Thus, a combination of Tsuji and Ito et al. would not produce Applicant's invention, as claimed in claim 26. Consequently, Applicant's invention, as claimed in claims 26, would not have been obvious to one of ordinary skill in the art of semiconductor packaging at the time the invention was made.

Applicant has amended claim 28. Claim 28 is dependent on claim 26. Claim 28, as amended, of the present invention claims the device of claim 26 further comprising the first line and the second line, wherein each segment of a bond pad is electrically connected to the first line and the second line.

Neither Tsuji nor Ito et al. teaches a device, as claimed in claim 26, as amended, of the present invention, including a first set of vias located over a first line and a second set of vias located over a second line wherein each segment of a bond pad is electrically connected to the first set of vias and the second set of vias.

Furthermore, neither Tsuji nor Ito et al. teaches a device, as claimed in claim 28, as amended, of the present invention, including the first line and the second line, wherein each segment of a bond pad is electrically connected to the first line and the second line.

Thus, a combination of Tsuji and Ito et al. would also not produce Applicant's invention, as claimed in claim 28. Consequently, Applicant's invention, as claimed in claims 28, would also not have been obvious to one of ordinary skill in the art of semiconductor packaging at the time the invention was made.

Since the two references cited by the Examiner do not teach, suggest, or render obvious claims 26 and 28 of Applicant's claimed invention, Applicant respectfully requests the Examiner to withdraw the rejections to claims 26 and 28 under 35 U.S.C. §103 (a).

Claim Rejections 35 U.S.C. § 103 (a)

Claims 1, 6-7, and 10-13

The Examiner has rejected claims 1, 6-7, and 10-13 under 35 U.S.C. §103 (a) as being unpatentable over Ezawa et al. (US 6,404,051) and Takeda et al. (JP 05-013418).

Applicant respectfully disagrees with the Examiner.

Applicant has amended claim 1. Claim 1, as amended, of the present invention claims a device having Input/Output (I/O) connections including: a bond pad (41B); a passivation layer located over the bond pad; vias (42N) located in the passivation layer to uncover the bond pad; a BLM located over the vias, the BLM split into two or more segments (44N), the segments in close proximity to each other, the segments separated by a gap, each of the segments connected to two or more of the vias; and a bump (45) located directly on the segments and in the vias. See Figure 4 and lines 10-12 on page 7 of the specification.

Applicant has also canceled claim 11 and amended claims 12-13.

However, neither Ezawa et al. nor Takeda et al. teaches a device including each of the segments of a BLM connected to two or more of the vias which uncover a bond pad.

Thus, a combination of Ezawa et al. and Takeda et al. would not produce Applicant's invention, as claimed in claim 1. Consequently, Applicant's invention, as claimed in claim 1 would not have been obvious to one of ordinary skill in the art of semiconductor packaging at the time the invention was made.

Claims 6-7 and 10-13 are dependent on claim 1, as amended.

Thus, a combination of Ezawa et al. and Takeda et al. would also not produce Applicant's invention, as claimed in claim 1. Consequently, Applicant's invention, as claimed in claim 1 would not have been obvious to one of ordinary skill in the art of semiconductor packaging at the time the invention was made.

Since the two references cited by the Examiner do not teach, suggest, or render obvious claim 1, as amended, of Applicant's claimed invention, Applicant respectfully requests the Examiner to withdraw the rejections to claims 1, 6-7, and 10-13 under 35 U.S.C. §103 (a).

Claims 2-4

The Examiner has rejected claims 2-4 under 35 U.S.C. §103 (a) as being unpatentable over Ezawa et al. (US 6,404,051) and Takeda et al. (JP 05-013418) as applied to claim 1 above, and in further view of Tadauchi et al. (US 6,464,122).

Applicant respectfully disagrees with the Examiner. Claims 2-4 are dependent on claim 1.

Applicant has amended claim 1. Claim 1, as amended, of the present invention claims a device having Input/Output (I/O) connections including: a bond pad (41B); a passivation layer located over the bond pad; vias (42N) located in the passivation layer to uncover the bond pad; a BLM located over the vias, the BLM split into two or more segments (44N), the segments in close proximity to each other, the segments separated by a gap, each of the segments connected to two or more of the vias; and a bump (45) located directly on the segments and in the vias. See Figure 4 and lines 10-12 on page 7 of the specification.

Applicant has also amended claim 4.

However, Ezawa et al., Takeda et al., and Tadauchi et al. do not teach a device including each of the segments of a BLM connected to two or more of the vias which uncover a bond pad.

Thus, a combination of Ezawa et al., Takeda et al., and Tadauchi et al. would not produce Applicant's invention, as claimed in claims 2-4. Consequently, Applicant's invention, as claimed in claims 2-4 would not have been obvious to one of ordinary skill in the art of semiconductor packaging at the time the invention was made.

Since the three references cited by the Examiner do not teach, suggest, or render obvious claims 2-4 of Applicant's claimed invention, Applicant respectfully

requests the Examiner to withdraw the rejections to claims 2-4 under 35 U.S.C. §103 (a).

Claims 5 and 8-9

The Examiner has rejected claims 5 and 8-9 under 35 U.S.C. §103 (a) as being unpatentable over Ezawa et al. (US 6,404,051) and Takeda et al. (JP 05-013418) as applied to claim 1 above, and in further view of Wark et al. (US 6,613,662).

Applicant respectfully disagrees with the Examiner. Claims 5 and 8-9 are dependent on claim 1.

Applicant has amended claim 1. Claim 1, as amended, of the present invention claims a device having Input/Output (I/O) connections including: a bond pad (41B); a passivation layer located over the bond pad; vias (42N) located in the passivation layer to uncover the bond pad; a BLM located over the vias, the BLM split into two or more segments (44N), the segments in close proximity to each other, the segments separated by a gap, each of the segments connected to two or more of the vias; and a bump (45) located directly on the segments and in the vias. See Figure 4 and lines 10-12 on page 7 of the specification.

However, Ezawa et al., Takeda et al., and Wark et al. do not teach a device including each of the segments of a BLM connected to two or more of the vias which uncover a bond pad.

Thus, a combination of Ezawa et al., Takeda et al., and Wark et al. would not produce Applicant's invention, as claimed in claims 5 and 8-9. Consequently, Applicant's invention, as claimed in claims 5 and 8-9 would not have been obvious to one of ordinary skill in the art of semiconductor packaging at the time the invention was made.

Since the three references cited by the Examiner do not teach, suggest, or render obvious claims 5 and 8-9 of Applicant's claimed invention, Applicant respectfully requests the Examiner to withdraw the rejections to claims 5 and 8-9 under 35 U.S.C. §103 (a).

Claims 14-15

The Examiner has rejected claims 14-15 under 35 U.S.C. §103 (a) as being unpatentable over Ezawa et al. (US 6,404,051) and Takeda et al. (JP 05-013418) as applied to claim 1 above, and in further view of Wong (US 6,577,017).

Applicant respectfully disagrees with the Examiner. Claims 14-15 are dependent on claim 1. See Figure 5.

Applicant has amended claim 1. Claim 1, as amended, of the present invention claims a device having Input/Output (I/O) connections including: a bond pad (41B); a passivation layer located over the bond pad; vias (42N) located in the passivation layer to uncover the bond pad; a BLM located over the vias, the BLM split into two or more segments (44N), the segments in close proximity to each other, the segments separated by a gap, each of the segments connected to two or more of the vias; and a bump (45) located directly on the segments and in the vias. See Figure 4 and lines 10-12 on page 7 of the specification.

However, Ezawa et al., Takeda et al., and Wong do not teach a device including each of the segments of a BLM connected to two or more of the vias which uncover a bond pad.

Thus, a combination of Ezawa et al., Takeda et al., and Wong would not produce Applicant's invention, as claimed in claims 14-15. Consequently, Applicant's invention, as claimed in claims 14-15 would not have been obvious to

one of ordinary skill in the art of semiconductor packaging at the time the invention was made.

Since the three references cited by the Examiner do not teach, suggest, or render obvious claims 14-15 of Applicant's claimed invention, Applicant respectfully requests the Examiner to withdraw the rejections to claims 14-15 under 35 U.S.C. §103 (a).

Conclusion

Applicant believes that all claims pending, including amended claims 1, 4, 12-13, 26, and 28, are now in condition for allowance so such action is earnestly solicited at the earliest possible date.

Pursuant to 37 C.F.R. 1.136(a)(3), Applicant hereby requests and authorizes the U.S. Patent and Trademark Office to treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time.

Should there be any additional charge or fee, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, please charge Deposit Account No. 02-2666.

If a telephone interview would in any way expedite the prosecution of this application, the Examiner is invited to contact the undersigned at (408) 720-8300.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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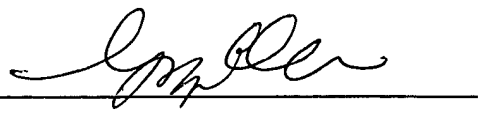

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